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PATENT

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : RICHARD W. FOOTE ET AL.
U.S. Serial No. : 10/777,012
Filed : February 11, 2004
For : SEMICONDUCTOR APPARATUS COMPRISING BIPOLAR
TRANSISTORS AND METAL OXIDE SEMICONDUCTOR
TRANSISTORS AND MANUFACTURING METHOD
Group No. : 2632
Examiner : Not Yet Assigned

MAIL STOP AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

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2. Information Disclosure Statement;
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4. Thirty-one (31) references.

relating to the above application, were deposited as "First Class Mail" with the United States Postal Service, addressed to, MAIL STOP AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 14, 2004.

Date: July 14, 2004

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Date: July 13, 2004

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Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Pursuant to the duty of disclosure under 37 C.F.R. § 1.56, Applicant submits this statement. This submittal is made in accordance with 37 C.F.R. §§ 1.97 and 1.98 and § 609 of the Manual of Patent Examining Procedure. The patents and publications herein are listed below and on the attached Forms PTO/SB/08A and PTO/SB/08B. Copy of the listed patents and publications are submitted herewith.

<u>U.S. Patent No.</u>	<u>Inventor</u>	<u>Date</u>
4,318,751	Hornig	March 9, 1982
4,545,087	Nahum	October 8, 1985
4,922,318	Thomas et al.	May 1, 1990
5,037,768	Cosentino	August 6, 1991
5,104,816	Verret et al.	April 14, 1992
5,141,891	Arima et al.	August 25, 1992
5,294,558	Subbanna	March 15, 1994
6,472,324	Kusakabe et al.	October 29, 2002

Publications

M. Shimizu et al., "A Novel Polysilicon Source/Drain Transistor with Self-Aligned Silicidation", LSI R&D Laboratory, Mitsubishi Electric Corporation, Pp. 11-12.

S. Hsia et al., "Polysilicon Oxidation Self-Aligned MOS (POSA MOS) - A New Self-Aligned Double Source/Drain Ion Implantation Technique for VLSI", IEEE Electron Device Letters, Vol. EDL-3, No. 2, February 1982, Pp. 40-42.

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C. S. Oh et al., "A New MOSFET Structure with Self-Aligned Polysilicon Source and Drain Electrodes", IEEE Electron Device Letters, Vol. EDL-5, No. 10, October 1984, Pp. 400-402.

W. Josquin et al., "The Integration of Double-Polysilicon NPN Transistors in an Analog BiCMOS Process", Extended Abstracts of the 20th (1988 International) Conference on Solid State Devices and Materials, Tokyo, 1988 Pp. 149-152.

Tunenori Yamauchi et al., "High Speed BICMOS Technology with Emitter-base Self-aligned Structure", Bipolar IC Division Fujitsu Limited, Pp. 155-158.

Kwang Soo Kim et al., "Bipolar-Complementary-Metal-Oxide-Semiconductor (BiCMOS) Technology with Polysilicon Self-Aligned Bipolar Devices", Japanese Journal of Applied Physics, Vol. 30, No. 10, October 1991, Pp. 2459-2465.

Masahiro Shimizu et al., "A Novel CMOS Structure with Polysilicon Source/Drain (PSD) Transistors by Self-Aligned Silicidation", IEICE Trans. Electron, Vol. E76-C, No. 4, April 1993, Pp. 532-540.

M. K. Moravvej-Farshi et al., "Novel Self-Aligned Polysilicon-Gate MOSFETS with Polysilicon Source and Drain, Solid-State Electronics, Vol. 30, No. 10, 1987, Pp. 1053-1062.

W. R. Burger et al., "An Advanced Self-Aligned BiCMOS Technology for High Performance 1-MegaBit ECL I/O SRAM's", National Semiconductor Corp., Puyallup Technology Development, 1989.

James Warnock et al., "BiCMOS Technology with 60-Ghz n-p-n Bipolar and 0.25- μ m CMOS", IEEE Electron Device Letters, Vol. 13, No. 11, November 1992, Pp. 578-580.

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T. Yuzuriha et al., "Submicron Bipolar-CMOS Technology Using 16 GHz f_T Double Poly-Si Bipolar Devices", Tektronix, Inc. IEEE 1988, Pp. 748-751.

T. Yoshimura et al., "0.6 μm High Speed BiCMOS Technology with Emitter-Base Self-Aligned Structure", Fujitsu Limited, Bipolar IC Division, IEEE 1989, Pp. 241-244.

K. G. Moerschel et al., "Best: A BiCMOS-Compatible Super-Self-Aligned ECL Technology", AT&T Microelectronics, AT&T Bell Laboratories, IEEE 1990 Custom Integrated Circuits Conference, Pp. 18.3.1-18.3.4.

Applicant hereby expressly reserves the right to swear behind the effective dates of any of the above Patents and to question the relevance and materiality of the Patents and Publications listed herein, in whole, in part, or in combination, subsequent to filing this Information Disclosure Statement.

Respectfully submitted,

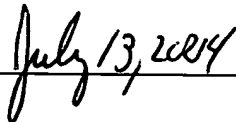
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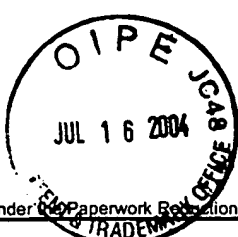
William A. Munck

Registration No. 39,308

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number	10/777,012
Filing Date	02/11/2004
First Named Inventor	Richard W. Foote
Art Unit	2632
Examiner Name	Not Yet Assigned
Attorney Docket Number	P05792

Sheet 1 of 4

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA	US- 4,318,751	03/09/1982	Hornig	
	AB	US- 4,545,087	10/08/1985	Nahum	
	AC	US- 4,922,318	05/01/1990	Thomas et al.	
	AD	US- 5,037,768	08/06/1991	Cosentino	
	AE	US- 5,104,816	04/14/1992	Verret et al.	
	AF	US- 5,141,891	08/25/1992	Arima et al.	
	AG	US- 5,294,558	03/15/1994	Subbanna	
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FOREIGN PATENT DOCUMENTS

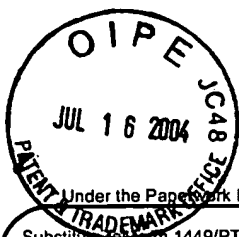
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Sheet 2 of 4

NON PATENT LITERATURE DOCUMENTS

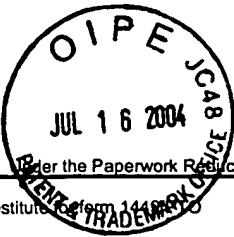
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	BA	M. Shimizu et al., "A Novel Polysilicon Source/Drain Transistor with Self-Aligned Silicidation", LSI R&D Laboratory, Mitsubishi Electric Corporation, Pp. 11-12.	
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Examiner Signature		Date Considered	
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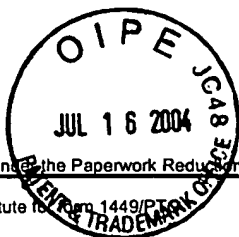
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CA	W. R. Burger et al., "An Advanced Self-Aligned BiCMOS Technology for High Performance 1-MegaBit ECL I/O SRAM's", National Semiconductor Corp., Puyallup Technology Development, 1989.	
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	DA	T. Yuzuriha et al., "Submicron Bipolar-CMOS Technology Using 16 Ghz ft Double Poly-Si Bipolar Devices", Tektronix, Inc. IEEE 1988, Pp. 748-751.	
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